

FPGA-Based Hardware Implementation for Torque Ripple Minimization in BLDC Drives

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ABSTRACT

Brushless DC motors have a trapezoidal back emf waveform and are fed with rectangular stator currents. On these conditions the torque produced is, theoretically, constant. However, in practice, torque ripple may exist, due to the machine itself but also to the feeding system. The causes of ripple coming from the machine are cogging torque and emf waveform imperfections. In this paper we discuss on the torque ripples minimisation by average torque control technique. Fpga is used for switching the Bldc motor and control. Coding on FPGA is done using the software Xilinx. The simulation is done using MATLAB. This method is not designed to reduce the torque ripple caused by high speed switching.

INTRODUCTION

BLDC motor are used in common now a days because of features like they have high efficiency, low maintenance and long life, low noise, control simplicity, low weight, and compact construction. That’s why the Bldc motor has become a very popular and viable product in the market. Actually the Bldc motor has more advantages compared with other types of AC motors in the market [1]. Fig. 1 shows the ideal and actual measured three-phase back EMF. The electromagnetic torque may be written as:

$$T_e = \frac{1}{\omega_m} (e_a i_a + e_b i_b + e_c i_c)$$

where ω_m is the mechanical angular velocity, e_a, e_b, e_c the three phase back EMFs and i_a, i_b, i_c the three phase currents.

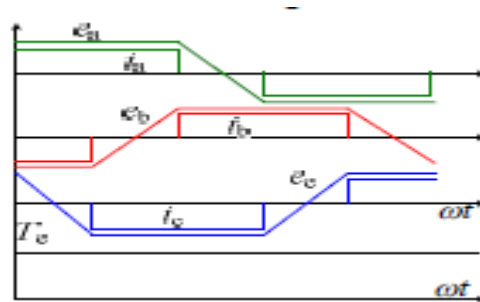


FIG 1: a) Ideal back EMF

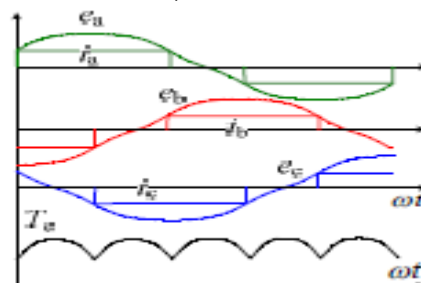


Fig 1:b :Actual measured back emf

According to (eqn 1), with ideal rectangular current, the electromagnetic torque is constant if the machine has an ideal trapezoidal back EMF, as shown in Fig. 1 (a). However, for the machine with non-ideal trapezoidal back EMF, such as the waveforms shown in Fig. 1 (b), the electromagnetic torque is not constant when the phase-current is still the rectangular waveform. Fig. 1(b) shows the torque waveform and the frequency of the torque ripple is six times the fundamental component of the back EMF.

WORKING OF PROPOSED ALGORITHM

The energy flowing into the system in one switching cycle dW_e is equal to the summation of energy change in the air-gap dW_m , the mechanical output energy dW_{mech} , and the system losses dW_{loss} :

$$dW_e = dW_m + dW_{mech} + dW_{loss}$$

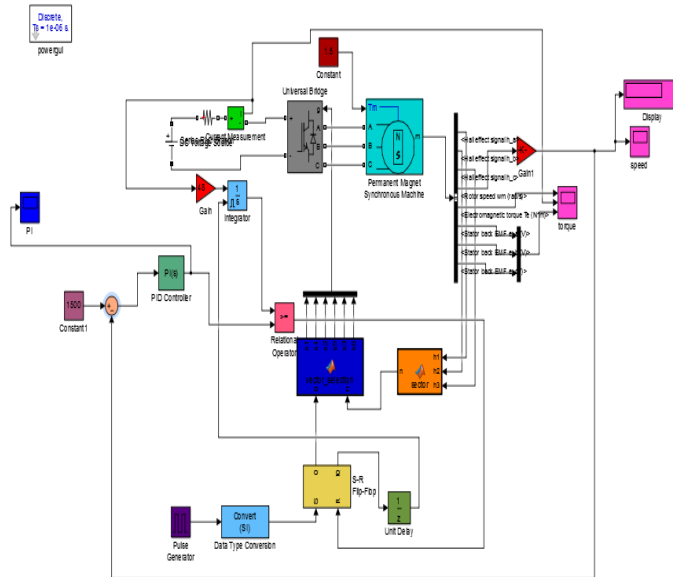


Fig 2: MATLAB simulation of the proposed system

$$dW_e = dW_{mech} + dW_{loss} = \frac{1}{\eta} dW_{mech}$$

where η is the efficiency of the system. The relationship between the input energy and the average torque T_{av} in one switching cycle can be expressed as:

$$dW_e = \frac{1}{\eta} dW_{mech} = \frac{\Delta\theta}{\eta} T_{av} = k T_{av}$$

$\Delta\theta$ is the mechanical angular position change in one switching cycle and k the coefficient defined as $\Delta\theta/\eta$ which is constant under the steady state. The electric machine torque variation will reflect as the DC input energy fluctuation. The average torque T_{av} may be computed by using the energy flowing into the system for each control cycle. The DC bus voltage and current are monitored by sensors. The input energy in one control cycle is calculated by integrating the product of the DC bus voltage and current.

FPGA

A field programmable gate array (FPGA) is a general-purpose integrated circuit that is programmed by the designer rather than the device manufacturer .FPGAs are high performance data processing devices. The raw memory bandwidth of a large FPGA running at a clock rate of 150 MHz can be hundreds of terabytes per second. An FPGA can be reprogrammed, even after it has been deployed into a system. An FPGA is programmed by downloading a configuration program called a bitstream into static on-chip random-access memory. Much like the object code for a microprocessor, this bitstream is the product of compilation tools that translate the high-level abstractions produced by a designer into something equivalent but low-level and executable. Xilinx System Generator is a powerful tool for compiling an FPGA program from a high-level Simulink model based design .

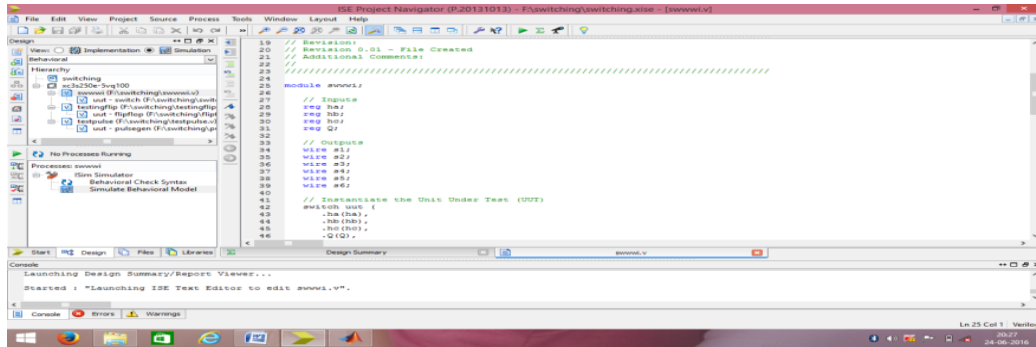


Fig 3: Coding of FPGA

STEP BY STEP PROCESS OF PROGRAMMING IN FPGA

- 1) Architectural Design
- 2) Choice of language (Verilog, VHDL)
- 3) Editing Programmes.
- 4) Compiling Programmes.
- 5) Synthesizing programs(.EDIF)
- 6) Placing and routing programs (.VO, .SDF, .TTF)
- 7) Loading programs to FPGA
- 8) Debugging FPGA programs
- 9) Documenting programs
- 10) Delivering programs

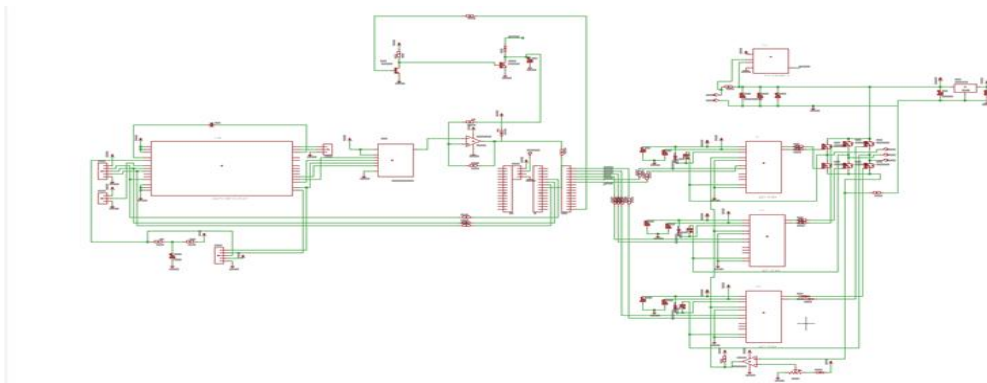
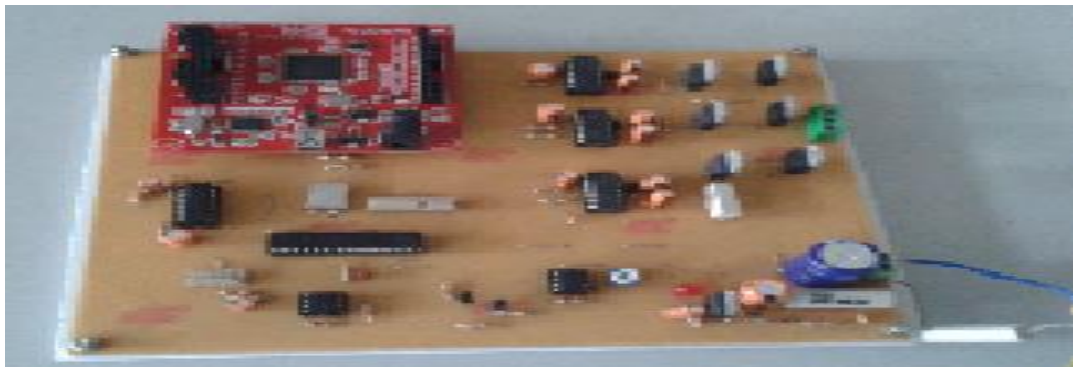


Fig 4:Hardware Schemat

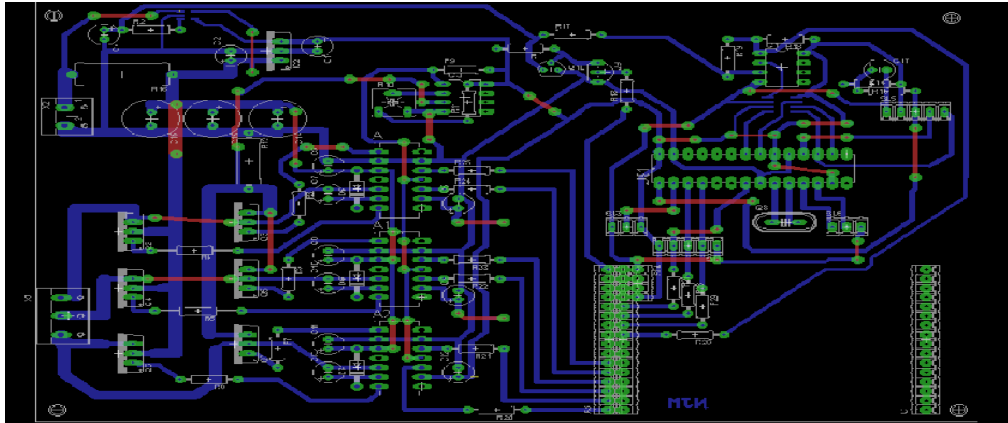


Fig 5:PCB Model

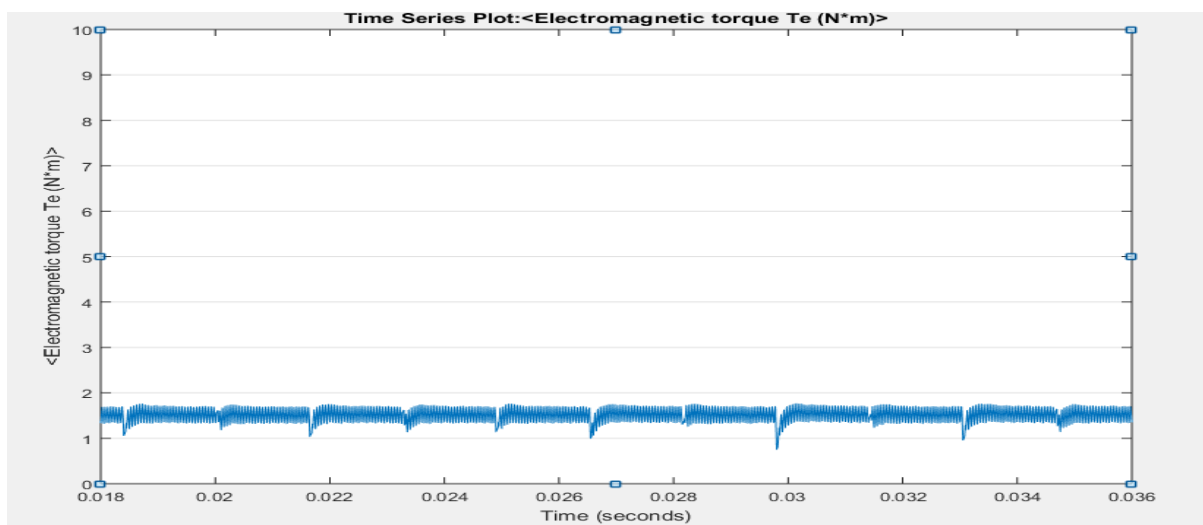


Fig 6:Electromagnetic torque of the proposed system

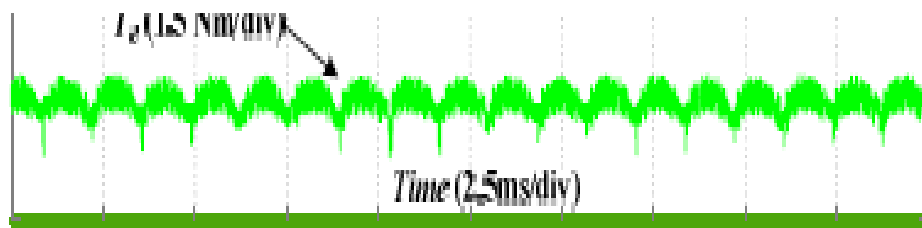


Fig 7:Electromagnetic torque from Conventional closed loop current control

Using the traditional control, the current is controlled to follow a square reference waveform and the torque shows the arc-shape ripple. The one-cycle torque control method ensures that the average torque in each switching cycle follows the reference. Thus to the controller can make sure the product of current and back EMF is constant. Arc shaped ripples are reduced. The current is not rectangular waveform and the torque is flat without the arc-shaped ripples. The proposed average torque control method is not designed to reduce the torque ripple caused by high speed switching.

CONCLUSION

The torque ripple spectrum analysis demonstrates the one-cycle average torque control algorithm is able to reduce the torque harmonic components by more than 70%. The approximate cost of hardware is twelve thousand rupees including the motor. This method does not require the information of back EMF and accurate rotor position. The one cycle torque control method ensures that the average torque in each switching cycle follows the reference. Thus to the controller can make sure the product of current and back EMF is constant. arc shaped ripples are reduced.

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